

Abstract of the Disclosure

The disclosure is a semiconductor memory device operable with a multi-sector erase mode for a multiplicity of memory chips, including a cell array, a register circuit containing information for a sector to be erased, an address clock driving circuit for contemporaneously generating an address clock signal from each memory chips, a counter for generating address signals in sequence, a core driver for executing an erase operation for the sector, and a control circuit thereof.

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